WHAT IS CLAIMED IS:

1. A memory module comprising a plurality of memory devices, which share a bus line, on a board,

wherein the bus line connects terminals of said plurality of memory devices in a stubless configuration and an end of said bus line is terminated.

2. The memory module as defined by claim 1 wherein at least a part of said bus line is a strip line.

3. The memory module as defined by claim 1 wherein an effective characteristic impedance of said bus line is matched with a characteristic impedance of a line on a motherboard on which said memory module is mounted.

4. The memory module as defined by claim 1

wherein at least one of said plurality of memory devices is a memory device in which a termination circuit is included and

wherein the memory device in which said termination circuit is included terminates the end of said bus line.

5. A memory module comprising a board on which a plurality of memory devices, which share a bus line, are mounted on at least one of a front surface and a back surface,

wherein said bus line is connected to one end of a strip line through a via hole on said board,

wherein terminals of said plurality of memory devices on said board are connected to said strip line each through a via hole, and

wherein another end of said strip line is terminated by being

connected to a termination circuit on the front surface of the board or the back surface of the board through a via hole or to a terminal of a memory device including a termination circuit.

6. The memory module as defined by claim 5 wherein the terminals of the memory devices on the front surface of the board and the terminals of the memory devices on the back surface of the board are connected alternately to said strip line each through a via hole.

7. The memory module as defined by claim 1 or 4 wherein said memory device comprises an on-chip terminator terminating said bus line by turning on a transfer gate that is provided between one end of a termination resistor and a termination voltage, the other end of the termination resistor being connected to the terminal of said memory device connected to said bus line.

8. The memory module as defined by claim 1 or 4

wherein said memory device comprises an on-chip terminator comprising a first transfer gate and a second transfer gate and terminating said bus line by turning on said first transfer gate and said second transfer gate,

wherein said first transfer gate is connected between one end of a first termination resistor and a high-potential power supply voltage, the other end of the first termination resistor being connected to the terminal of said memory device connected to said bus line and

wherein said second transfer gate is connected between one end of a second termination resistor and a low-potential power supply voltage, the other end of the second termination resistor being connected

to the terminal of said memory device connected to said bus line.

9. A memory module comprising a board on which a plurality of memory devices, which share a bus line, are mounted on a front surface and a back surface,

wherein said bus line is extended on the front surface of said board from a first module terminal to a via hole spaced from said first module terminal and is connected to one end of a first strip line through the via hole,

wherein terminals of the memory devices mounted on the front surface of the board are connected to said first strip line each through a via hole,

wherein said first strip line is extended in one direction and the other end, which is an end opposite to said one end, is connected to one end of a second strip line through a loop-back via hole,

wherein said second strip line is extended in a direction opposite to said one direction,

wherein terminals of the memory devices mounted on the back surface of the board are connected to said second strip line each through a via hole,

wherein a termination circuit is provided near a second module terminal on the back surface of the board, and

wherein said termination circuit is connected through a via hole to the other end of said second strip line that is looped.

10. The memory module as defined by claim 9 wherein, near a loop-back point of said bus line, a power supply layer and a ground layer,

between which said strip line forming said bus line is provided, are connected by a bypass capacitor and/or common power supply layers or ground layers are shorted.

11. The memory module as defined by claim 1 wherein signal terminals of said plurality of memory devices connected in the stubless configuration are connected at one point on the bus.

12. A memory module comprising a board on which a plurality of memory devices, which share a bus line, are mounted on a front surface and a back surface,

wherein said bus line is extended on the front surface of said board from a first module terminal to a via hole spaced from said first module terminal and is connected to one end of a strip line through the via hole and the other end of said strip line is connected through a via hole to a termination circuit provided on the front surface or back surface of the board and

wherein, for each of two memory devices mounted in opposing positions on the front surface and back surface of the board, said strip line is connected to terminals of said two memory devices each through a via hole extended from one position on said strip line to the front surface and the back surface.

13. A memory module comprising a board on which a plurality of memory devices, which share a bus line, are mounted on a front surface and a back surface,

wherein said bus line is extended on the front surface of said board from a first module terminal to a via hole spaced from said first

module terminal and is connected to one end of a first strip line through the via hole,

wherein said first strip line is extended in one direction and the other end, which is an end opposite to said one end, is connected to one end of a second strip line through a loop-back via hole,

wherein said second strip line is extended in a direction opposite to said one direction,

wherein a termination circuit is provided near a second module terminal on the back surface of the board,

wherein said termination circuit is connected to the other end of said second strip line through a via hole, and

wherein, for each of two memory devices mounted in opposing positions on the front surface and back surface of the board, said first strip line or said second strip line is connected to terminals of said two memory devices each through via hole extended from one point on said first strip line or said second strip line to the front surface and back surface of the board.

14. The memory module as defined by claim 13, wherein, for said plurality of memory devices mounted on the board, said first strip line and said second strip line are connected to the terminals of said memory devices through via holes extended alternately from said first strip line and said second strip line to the front surface of the board and the back surface of the board.

15. The memory module as defined by claim 1 wherein a register, connected to said bus line for converting signals, is provided on the

board of said memory module.

16. A memory module comprising a board on which a plurality of memory devices, which share a bus line, are mounted on a front surface and a back surface,

wherein said bus line is extended on the front surface of said board from a first module terminal to a via hole spaced from said first module terminal and is connected to one end of a first strip line through the via hole, the other end of said first strip line is connected to an input terminal of a signal conversion register on the front surface of the board through a via hole, an output terminal of the signal conversion register is connected to one end of a second strip line through a via hole, and the other end of said second strip line is connected to one end of a third strip line through a third via hole provided for looping back the line,

wherein said third strip line is extended in a direction opposite to the direction of said second strip line,

wherein a termination circuit is provided near a second module terminal on the back surface of the board, and

wherein said termination circuit is connected to the other end of said third strip line through a via hole.

17. The memory module as defined by claim 1

wherein said memory devices each have a package board that makes an electrical connection between a memory chip pad and said board and

wherein said package board has a strip line for use as a signal line of said bus line in said package board.

18. The memory module as defined by claim 1 wherein said memory module is configured as a multi-chip module.

19. The memory module as defined by one of claims 1-17 wherein the board of said memory module is divided into a plurality of boards and said plurality of boards are each connected by inter-board connection means.

20. A memory module wherein a memory module board on which a plurality of memory devices, which share a bus line, are mounted on a front surface and a back surface is divided into at least two boards that are interconnected by inter-board connection means,

wherein a first board, which is one of said two boards, is connected to a motherboard through a connector, said bus line is connected to one end of a first strip line through a via hole on said first board, terminals of memory devices mounted on a front surface of said first board are connected to said first strip line each through a via hole, and the other end of said first strip line is connected to a second board through a via hole and said inter-board connection means,

wherein said bus line is connected to one end of a second strip line through a via hole on said second board and terminals of memory devices mounted on a front surface of said second board are connected to said second strip line each through a via hole,

wherein the other end of said second strip line is connected to one end of a third strip line through a via hole provided for loop-back and terminals of memory devices mounted on a back surface of said second board are connected to said third strip line each through a via

hole,

wherein the other end of said third strip line is connected to said first board through a via hole and said inter-board connection means, and

wherein said bus line is connected to one end of a fourth strip line via a via hole on said first board, terminals of memory devices mounted on a back surface of said first board are connected to said fourth strip line each through a via hole and the other end of said fourth strip line is connected to a termination circuit on the board through a via hole.

21. The memory module as defined by one of claims 1-18

wherein said memory device and/or a register mounted on said memory module and connected to said bus line has an input terminal and an output terminal, instead of a two-way input/output terminal, for at least one two-way signal of said bus line and

wherein said bus line has a one-way input signal line and a one-way output signal line, connected respectively to said input terminal and said output terminal, instead of a two-way signal line.

22. A memory module having a plurality of memory devices, which share a bus line, on a front surface and a back surface of a board,

wherein said memory device and/or a register mounted on said memory module and connected to said bus line has an input terminal and an output terminal, instead of a two-way input/output terminal, for at least one two-way signal of said bus line,

wherein said bus line has a one-way input signal line and a

one-way output signal line, connected respectively to said input terminal and said output terminal, instead of a two-way signal line,

wherein a one-way first signal line is connected to one end of a first strip line through a via hole on said board, and the input terminal of the memory device mounted on the front surface and/or the back surface of said board is connected to said first strip line through a via hole, and

wherein a one-way second signal line is connected to one end of a second strip line through a via hole and the output terminal of the memory device mounted on the front surface and/or the back surface of said board is connected to said second strip line through a via hole.

23. A memory system having at least one memory module each of which has a plurality of memory devices on a front surface and/or a back surface of a board and has a bus line at least part of which is wired using a strip line embedded between a power supply layer and a ground layer in said board and whose end is terminated by a termination circuit provided on said board,

wherein said memory module is mounted on a motherboard via a connector, said motherboard having a memory controller sending and receiving a command/address signal and a data signal to or from said memory module, and

wherein said memory module uses, for one data signal, said strip line to connect data terminals of said plurality of memory devices in a stubless configuration and an effective characteristic impedance of said bus line is matched with a characteristic impedance of a line in said motherboard.

24. The memory system as defined by claim 23,

wherein the bus line extended from one side of said board, on which a plurality of module terminals are provided, to the other side, which is opposite to said one side of said board, is extended from said one side of the board to the other side using the strip line, the end of the strip line on said other side is looped back through a via hole, and a terminating device is provided near a termination terminal.

25. A memory system comprising:

said memory module as defined by one of claims 1-22 wherein said bus line of said memory module includes a bus line for a data signal; and

a memory controller that sends a command/address signal to said memory device of said memory module and transfers the data signal to and from said memory device,

wherein data lines between said memory controller and slots are connected in a point to point configuration.

26. The memory system as defined by claim 25 wherein at least a part of said data lines between said memory controller and the slots is a strip line.

27. The memory system as defined by claim 25 wherein a shield is provided between each two data lines.

28. The memory system as defined by claim 25 wherein at least one signal line, which connects said memory controller and two slots in a T-branch structure, is included.

29. The memory system as defined by claim 28 wherein said signal

line is a command/address signal line.

30. The memory system as defined by claim 25 wherein said data line is terminated by both said memory controller and said memory module.

31. The memory system as defined by claim 25 wherein one channel is divided into a plurality of slots.

32. The memory system as defined by claim 25 wherein said memory module has a memory device, which contains a termination circuit, on a board, wherein two memory devices mounted across said board and placed in opposing positions on a front surface of said board and a back surface of said board are connected commonly to said bus line, and wherein said bus line is terminated by one of said two devices which is not accessed or driven.

33. The memory system as defined by claim 25 wherein a reference voltage (Vref) is generated by said memory controller and the memory device that terminates the bus line.

34. The memory system as defined by claim 25

wherein said memory module is connected to a motherboard via said connector, said motherboard having said memory controller mounted thereon and

wherein said connector is a butterfly type connector with a configuration in which said memory module is inserted in a direction parallel to a surface of said motherboard.

35. The memory system as defined by claim 25

wherein said memory module is connected to a motherboard via said connector, said motherboard having said memory controller

mounted thereon and

wherein said memory module and/or said connector has cooling means.

36. The memory system as defined by claim 25 wherein said memory controller has a logical threshold voltage output circuit that generates a reference voltage,

wherein the reference voltage output from said logical threshold voltage output circuit is connected to said memory module via a reference voltage line,

wherein, in said memory module, an on-chip terminator on the memory device that includes a termination circuit at the end of said bus line is connected to said reference voltage line,

wherein a reference voltage terminal of the memory device connected to said bus line is connected to said reference voltage line, and

wherein said logical threshold voltage output circuit has a push-pull type driver circuit with the same configuration as that of a push-pull type driver circuit in an output circuit and an input terminal and an output terminal of said push-pull type drive circuit are connected.

37. The memory system as defined by claim 25 wherein said memory controller has a logical threshold voltage output circuit that generates a reference voltage,

wherein the reference voltage output from said logical threshold voltage output circuit is connected to said memory module via

a reference voltage line,

wherein, in said memory module, an on-chip terminator on the memory device that includes a termination circuit at the end of said bus line is connected to said reference voltage line,

wherein a reference voltage terminal of the memory device connected to said bus line is connected to said reference voltage line,

wherein said memory controller has an output circuit comprising an open drain type driver,

wherein a gate terminal of said open drain type driver is connected to an output terminal of a level conversion circuit that receives an internal signal and that performs level conversion,

wherein said logical threshold voltage output circuit has the level conversion circuit which has the same configuration as that of said output circuit and in which an input terminal and an output terminal are connected, and

wherein an output of said level conversion circuit is connected to a gate terminal of said open drain type driver for outputting the reference voltage.

38. The memory system as defined by claim 25 wherein registers are provided on a motherboard, each of said registers being connected to said bus line for performing signal conversion.

39. The memory system as defined by claim 25

wherein said memory device and/or a register mounted on said memory module and connected to said bus line has an input terminal and an output terminal, instead of a two-way input/output terminal, for at

least one two-way signal of said bus line,

wherein said bus line has a one-way input signal line and a one-way output signal line connected respectively to said input terminal and said output terminal of said memory device or said register,

wherein said memory controller on a motherboard has an output terminal and an input terminal corresponding to signals from the input terminal and the output terminal of said memory device or said register, and

wherein said output terminal and said input terminal of said memory controller are connected respectively to said input terminal and said output terminal of said memory device and/or said register each via said one-way line in a point-to-point configuration.

40. The memory system as defined by claim 25 wherein said memory device and/or a register mounted on said memory module and connected to said bus line has an input terminal and an output terminal separately, instead of having one input/output terminal, for at least one two-way signal of said bus line,

wherein said bus line has a one-way input signal line and a one-way output signal line connected respectively to said input terminal and said output terminal of said memory device or said register,

wherein said memory controller on a motherboard has an output terminal and an input terminal corresponding to signals from the input terminal and the output terminal of said memory device or said register, and

wherein a daisy chain connection is made between said memory

controller and the slots of a plurality of said memory modules via said one-way input signal line and output signal line.

41. The memory system as defined by claim 25

wherein said memory device and/or a register mounted on said memory module and connected to said bus line has an input terminal and an output terminal separately, instead of having one input/output terminal, for at least one two-way signal of said bus line,

wherein said bus line has a one-way input signal line and a one-way output signal line connected respectively to said input terminal and said output terminal of said memory device or said register,

wherein said memory controller on a motherboard has an output terminal and an input terminal corresponding to signals from the input terminal and the output terminal of said memory device or said register,

wherein said output terminal or said input terminal of said memory controller is connected respectively to said input terminal or said output terminal of a memory device mounted on said memory module in a slot at a starting position and/or said register via said one-way line,

wherein, between said memory modules, the output terminal and the input terminal of said memory device in one slot and/or said register are connected respectively to the input terminal and the output terminal of said memory device in a neighboring slot and/or said register through a connector and one-way lines, and

wherein the output terminal or the input terminal of said memory device in a slot at an ending position and/or said register is

connected to said input terminal or said output terminal of said memory controller via said one-way line of said motherboard.

42. The memory system as defined by claim 25 wherein said memory device and/or a register mounted on said memory module and connected to said bus line differentially transmits at least one signal of said bus line to or from said memory controller on a motherboard connected via a connector.

43. The memory system as defined by claim 42

wherein, in said bus line, at least one line pair out of a plurality of line pairs, over which the signal is differentially transmitted, is composed of a first line and a second line which are complementary each other and are placed in this order in a connection from said memory controller to said connector and

wherein the positions of the first line and the second line of said line pair are exchanged and said lines are placed in order of said second line and said first line in a connection from said connector and said memory module.

44. The memory system as defined by claim 42

wherein, for said plurality of line pairs, a first line pair and a second line pair are alternately placed, said first line pair being composed of complementary signals whose positions are exchanged between a connection from said memory controller to said connector and a connection from said connector to said memory module, said second line pair being composed of complementary signals whose positions are not exchanged between the connection from said memory controller to

said connector and the connection from said connector to said memory module.